Taping out Complex SOC

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SoC – The Pace is Fast and Getting Faster

<table>
<thead>
<tr>
<th>iPhone</th>
<th>iPhone 3GS</th>
<th>iPhone 4</th>
<th>iPhone 4S</th>
<th>Iphone 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>620MHz / 128Mb</td>
<td>620MHz/256Mb</td>
<td>800MHZ / 512Mb</td>
<td>800MHZ/512MB</td>
<td>?</td>
</tr>
<tr>
<td>2 Mega pixel camera</td>
<td>3 Mega Pixel Camera</td>
<td>5 Mega Pixel Camera, A4 Chip</td>
<td>8 Mega Pixel Camera, Dual Core A5 Chip</td>
<td>?</td>
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Design Challenges of the Latest Generation SOC’s

A State-of-the-Art Mobile Application Processor

- Multi-Core ARM Processors
- Multi-Core 3D-Graphics GPU
- HD Multimedia & Image Processor
- USB & I/O
- Audio/Video DSP
- Memory & Storage Subsystem
- 4G/3G/2G Modem
- WLAN Bluetooth GPS

All these complex IPs wrapped up in extreme LP top-level SoC implementation with liberal usage of DVFS
Complex SOC Styles Emerging

Channel-Based

Near-Abutted

Fully-Abutted

Repeated Blocks

MVDD
Challenges in Complex SOC’s

• High Performance
  – Competitive performance area and power
  – Concurrent multi mode multi corner optimization and analysis

• Low Power
  – Comprehensive multi VDD and low leakage solutions
  – DVFS through MM/MC analysis and optimization

• High Capacity
  – Designs are getting bigger and bigger

• High reliability
  – High redundant via ratio, advanced wire jogging etc

• High Flexibility
  – Ability to easily tune flow for specific end user needs
Toolset for taping out Complex SOC.

- **Talus Design**
  - RTL Synthesis
  - DFT, LBIST, MBIST.

- **HYDRA/FX**
  - Chip Planning & Prototyping

- **Talus Power Pro**
  - Power optimizer (Leakage, Clock Gating etc)

- **Talus Vortex**
  - Physical Synthesis
  - Clock Tree Synthesis
  - Routing

- **Third Party tools**
  - Formal Verification
  - ATPG
Managing Monster SOC – Magma Way

100M Cells

Cost
Schedule
Resources
Power
Productivity Must Improve

- Typical large semi company wish list

<table>
<thead>
<tr>
<th></th>
<th>2011</th>
<th>2013</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complexity</td>
<td>20M cells</td>
<td>40M cells</td>
<td>55M cells</td>
</tr>
<tr>
<td>TAT</td>
<td>3 ~ 4 months</td>
<td>3 ~ 4 months</td>
<td>3 ~ 4 months</td>
</tr>
<tr>
<td>Resources</td>
<td>3</td>
<td>3</td>
<td>3</td>
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</tbody>
</table>

- Conclusion
  - Designer throughput must increase (cells/day)
  - Designer capacity (block size) must increase
Today’s Approach

- Manually break the design into blocks of ~1M cells
- Make the right choices when slicing and dicing!
- Have lots of designers on hand! (not to mention loads of machines and software!)
- Be patient and have lots of $$ to spend!

How are we going to get past this?
An Idea – Leverage the Power of Hardware

- Automatically break the design into blocks
- Hardware does the work (multi-threading helps!)
- Powerful hardware is available; Complex software is the challenge...
Distributed Smart Sync™ Technology – Talux Vortex FX

**Distribute**

- Large design block

**Synchronize**

- Multi-Core Server Talus 1.2
- Multi-Core Server Talus 1.2
- Multi-Core Server Talus 1.2

**Talus Vortex FX**
High Capacity Design Methodology – End Result

MegaChip Design (~20M – 100M cells)

Partition

~ 4M – 10M cell partitions

Implement

Parallel implementation – server farm

Completed MegaChip

~ 20M – 100M cells
Managing Monster SOC – Magma Way

100M Cells

Power
The Cost of Pessimism in Power Measurement

Data Center

Orders of Magnitude

Single Core

Pessimistic optimization: ~250mW
ACCURATE optimization: ~200mW
Penalty: 50mW

Multi-Core

Penalty: 2.5W

Penalty in MEGAWATTS!

Multi-Core designs multiply the cost of missing opportunities for power reduction

ENGINEERING SUSTAINABLE SOLUTIONS

INDICON 2011
Key Power Management Challenges

- Higher Frequencies
- Voltages not decreasing
- Thermal Design Point (TDP)
- Reduced Form Factors
- Maintaining Productivity
- Verification

ENGINEERING SUSTAINABLE SOLUTIONS
Managing the Dynamic Power Problem

- Higher Frequencies
- Voltages not decreasing
- Maintaining Productivity
- Verification
- Thermal Design Point (TDP)
- Reduced Form Factors

Reduce Activity
Globally & Locally

Minimize Cell Switching Cap

Minimize RC for Highly Active Nets
Managing Power Productivity

Finding Gating Opportunities
- Automate the Search
- Automate the Verification

Code Management
- Operate at Netlist level
- Automate the Verification

Flow Methodology
- Fit into existing flow
- Maximize Benefits

- Higher Frequencies
- Voltages not decreasing

Factors
- Maintaining Productivity
- Verification

ENGINEERING SUSTAINABLE SOLUTIONS
Advanced Combinational Techniques – Reducing Activity

Traditional Clock Gating
- Rule based

```
always @ (posedge clk)
    if (enable) q <= d;
```

Multi-net Clock Gating
- Generates complex enables
- Considers many groupings
- Effective on control logic

Confidential - Do Not Duplicate
Looks ahead in future cycles ...

- Gates when value not used in future
- Effective both on data path and control logic
- Looks ahead many cycles
Complex Floor plans Evolving to reduce Voltage

- **Always On Domains**
- **Multi Voltage Domains**
- **Switchable/Shutoff Domains**
- **Variable voltage domains**
(Low) Power is King

- Designers need to continually strive to **Reduce** both **Operating** and **Quiescent Power**
- **Speed** and **Performance** needs to keep pace
- The answer lies in **Smart Low Power Technologies**
  - Leveraging the best MMMC architecture to optimal effect
- And Delivering these in a way that **Does Not affect Productivity**
  - And ultimately enhances it ......
Summary

• Taping out Monster SOC requires latest and smartest Technology.
• New way of thinking and implementation required for next generation technologies
• Magma lead the way in 28nm and 20nm production designs across customers